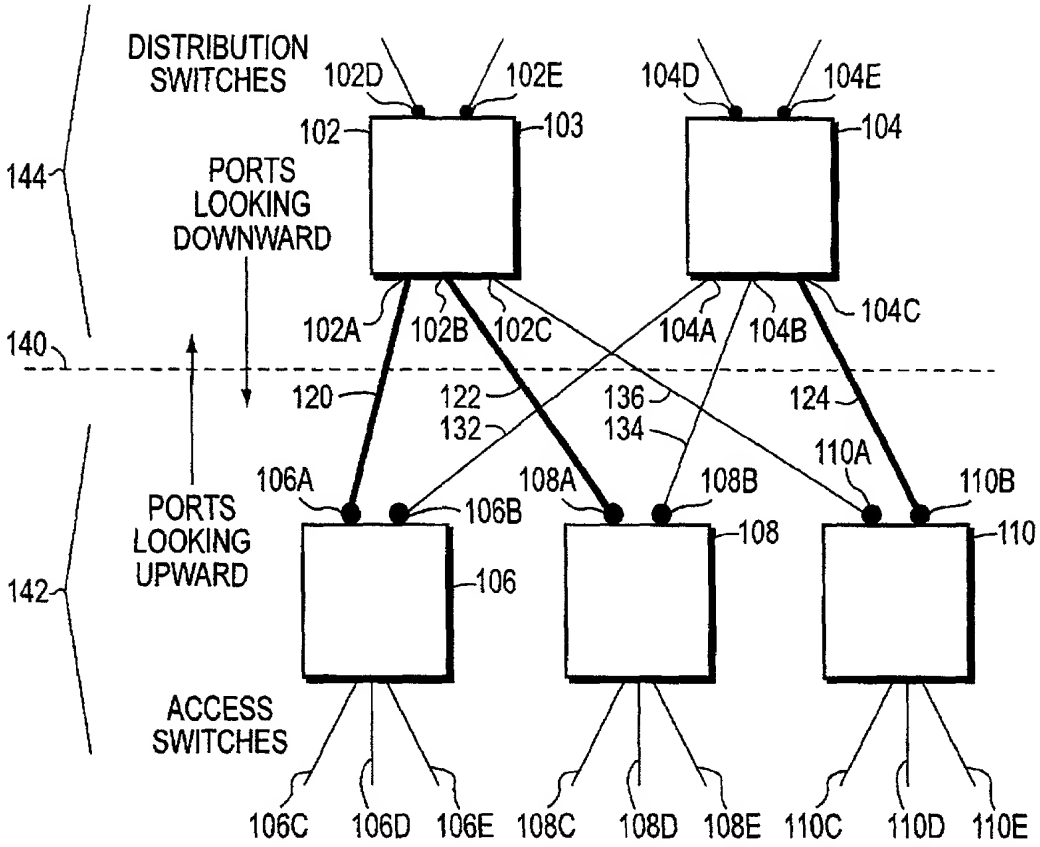

DISTRIBUTION SWITCHES
102D
102E
104D
104E
102
103
104
144
PORTS LOOKING DOWNWARD
102A
102B
102C
104A
104B
104C
140
120
122
136
124
132
134
110A
106A
108A
108B
110B
106B
108
110
PORTS LOOKING UPWARD
142
106
ACCESS SWITCHES
106C
106D
106E
108C
108D
108E
110C
110D
110E

FIG. 1

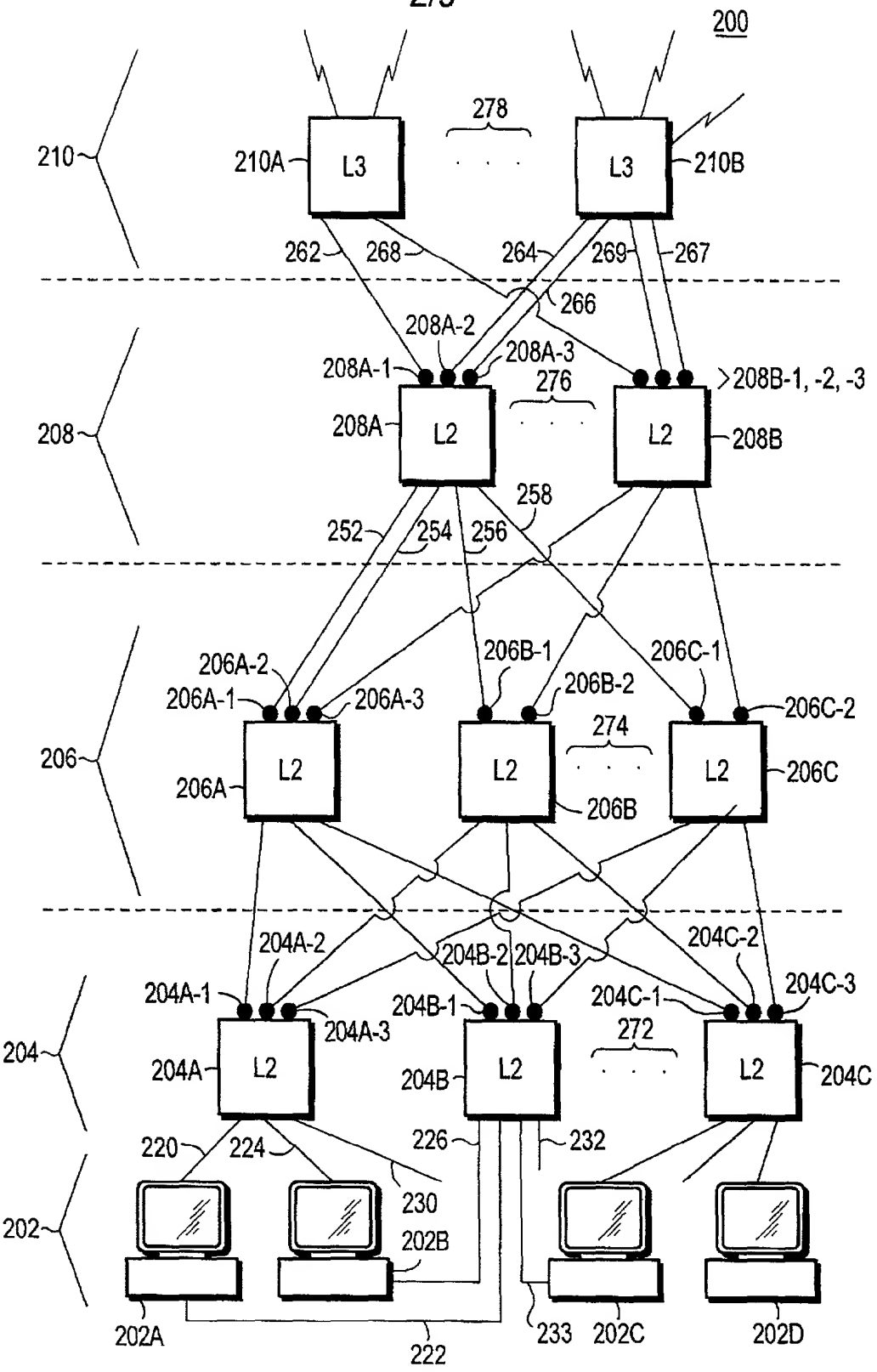
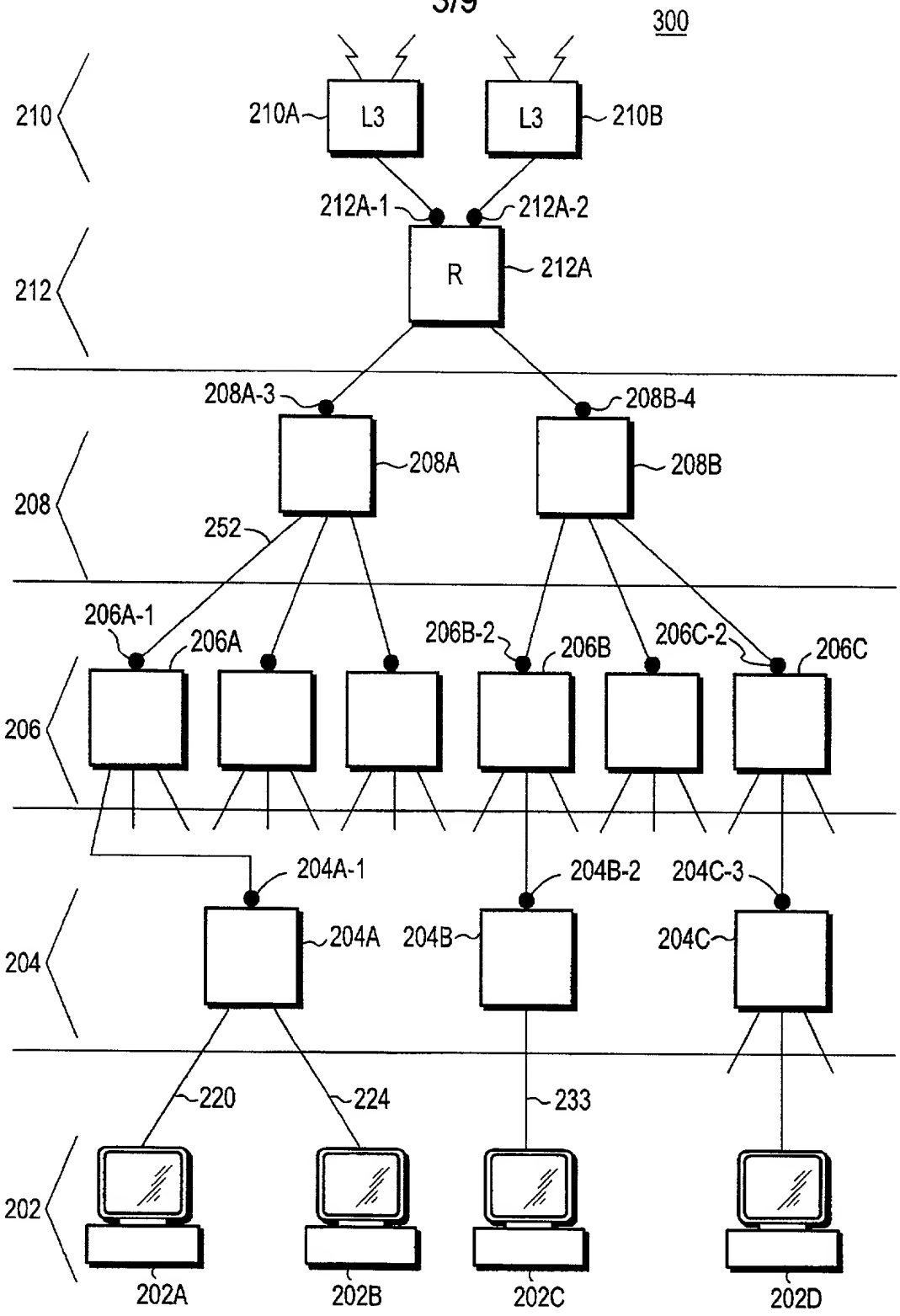

200
278
210
210A
L3
L3
210B
262
268
264
269
267
266
208A-2
208A-1
208A-3
276
208B-1, -2, -3
208
208A
L2
L2
208B
258
252
254
256
206A-2
206A-1
206A-3
206B-1
206B-2
206C-1
206C-2
206
274
206A
L2
L2
L2
206C
206B
204A-2
204B-2
204B-3
204C-2
204A-1
204B-1
204C-1
204C-3
204
272
204A
L2
204B
L2
L2
204C
220
224
226
232
230
202
202B
202A
222
233
202C
202D

FIG. 2



STP LOGICAL TREE

FIG. 3

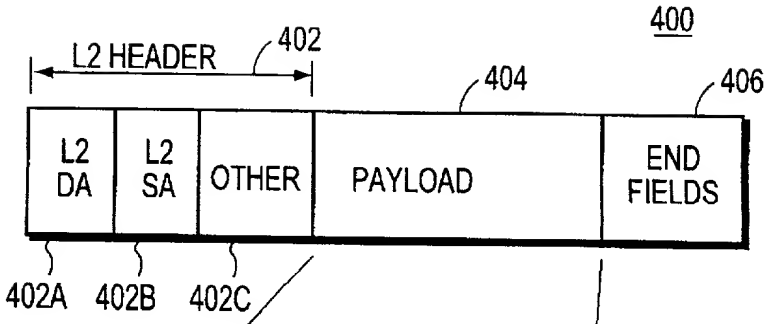


FIG. 4

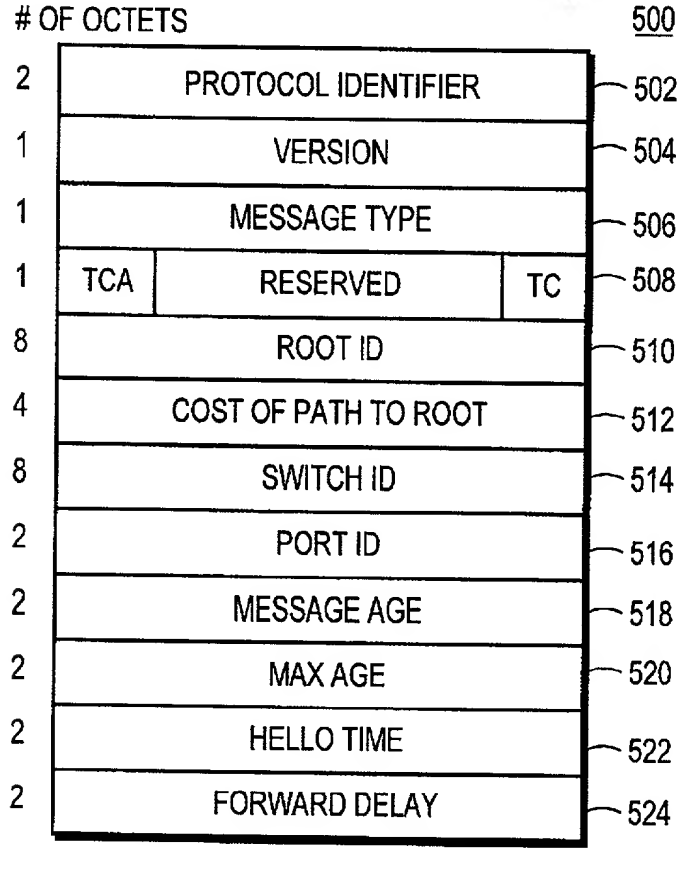
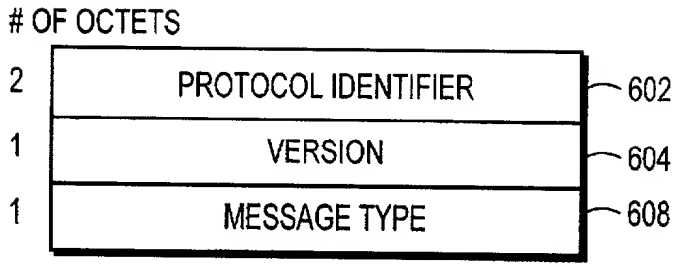


FIG. 5

CONFIGURATION MESSAGE

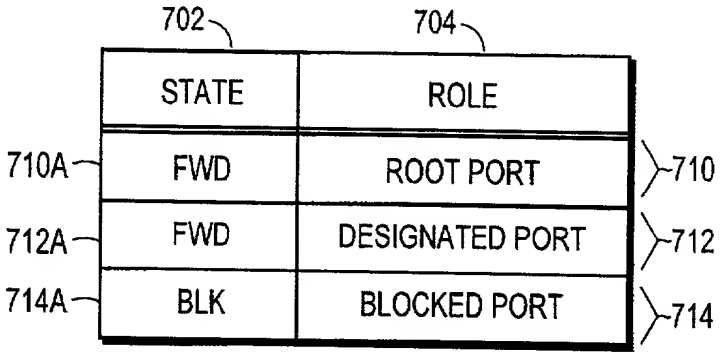
600



TOPOLOGY CHANGE NOTIFICATION MESSAGE

FIG. 6

700



PORT STATE TABLE
PRIOR ART

FIG. 7

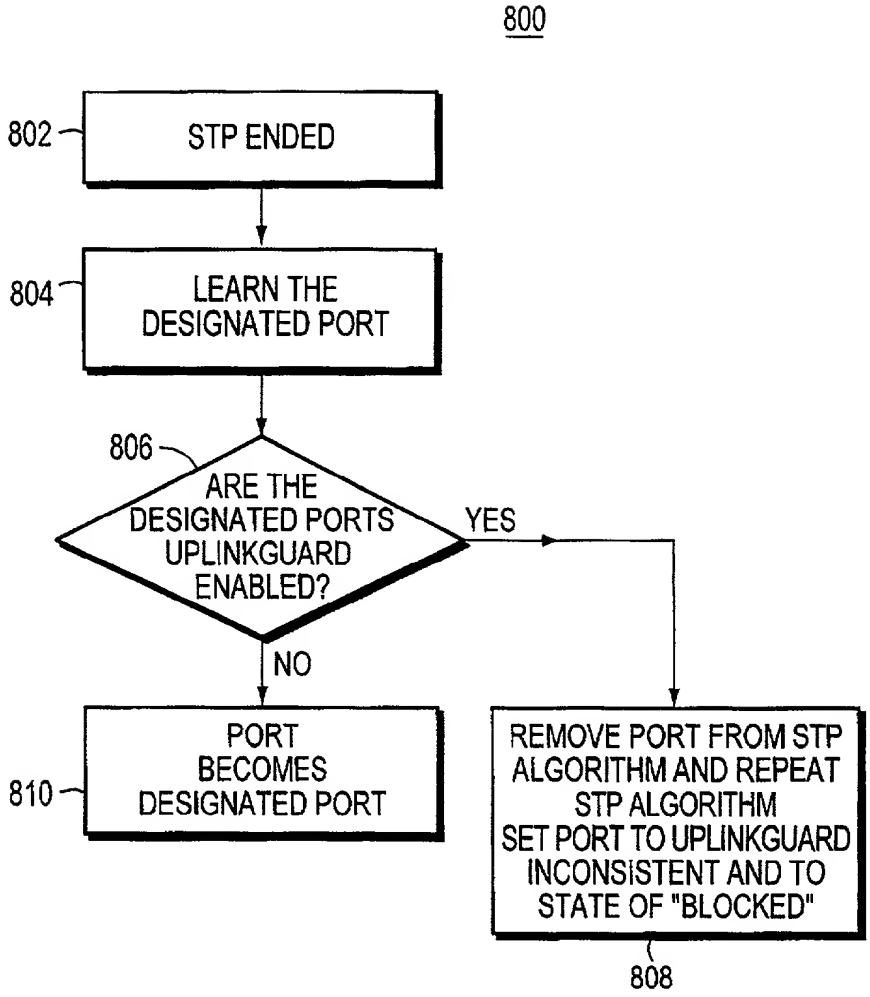

800
802
STP ENDED
804
LEARN THE DESIGNATED PORT
806
ARE THE DESIGNATED PORTS UPLINKGUARD ENABLED?
YES
NO
810
PORT BECOMES DESIGNATED PORT
REMOVE PORT FROM STP ALGORITHM AND REPEAT STP ALGORITHM SET PORT TO UPLINKGUARD INCONSISTENT AND TO STATE OF "BLOCKED"
808

FIG. 8

9,000

	910 STATE	912 ROLE	913 UPLINKGUARD ENABLED
914	FWD	ROOT PORT	DON'T CARE
916	FWD	DESIGNATED PORT	NO
918	BLK	BLOCKED PORT	DON'T CARE
920	BLK	UPLINK GUARD ENABLED BACKUP FOR ROOT PORT	DON'T CARE
922	UPLINKGUARD INCONSISTENT = BLK	DESIGNATED	YES

PORT STATE TABLE

FIG. 9

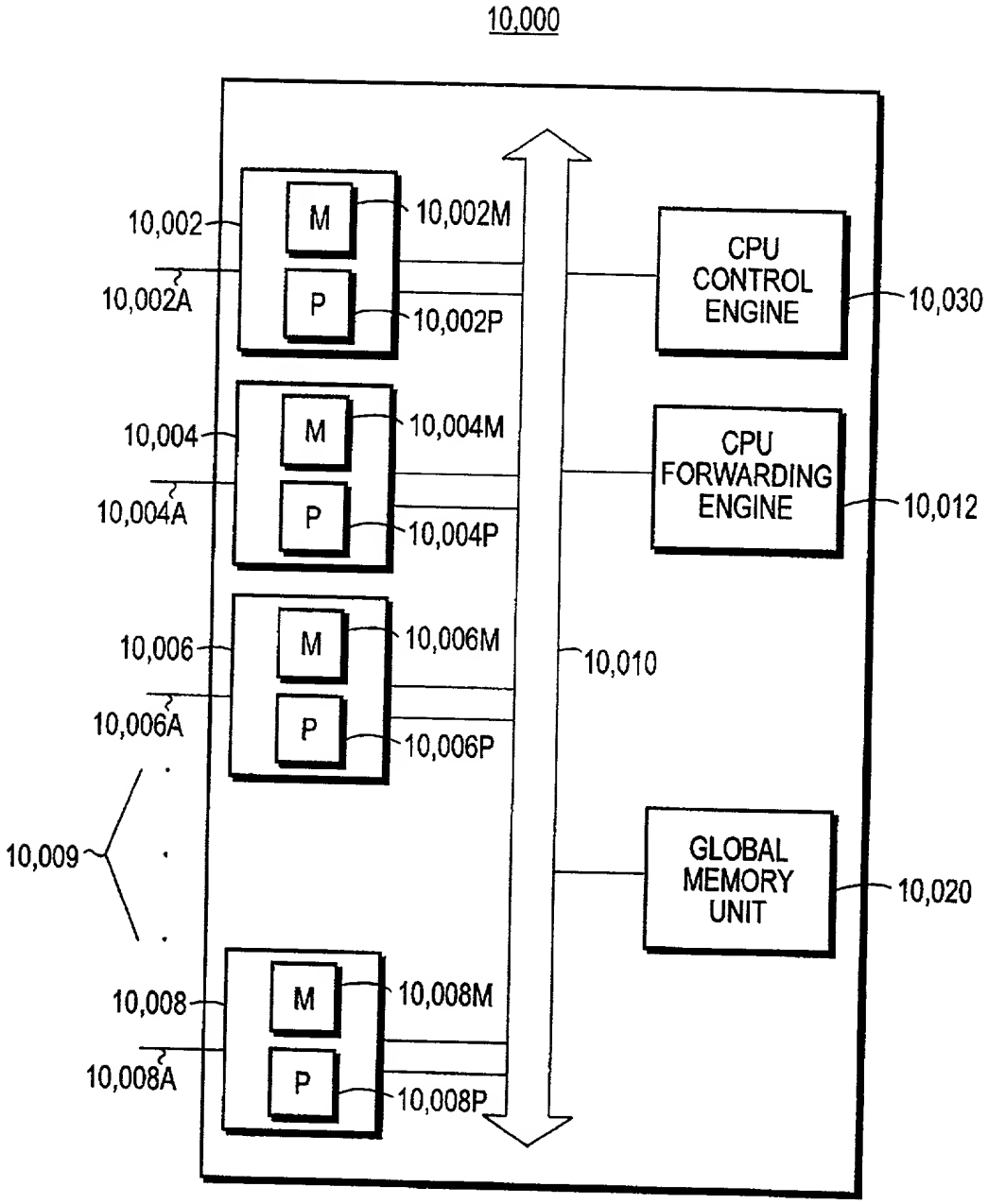

10,000
10,002
10,002A
M
P
10,002M
10,002P
10,004
10,004A
M
P
10,004M
10,004P
10,006
10,006A
M
P
10,006M
10,006P
10,009
10,008
10,008A
M
P
10,008M
10,008P
10,010
CPU CONTROL ENGINE
10,030
CPU FORWARDING ENGINE
10,012
GLOBAL MEMORY UNIT
10,020

FIG. 10